

Large area detectors and new sensor technologies at Fairchild Imaging

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ABSTRACT

In this paper, we present an overview of large area detector arrays and new sensor technologies currently under development at Fairchild Imaging. We discuss on-going development efforts aimed at satisfying the increasing need for large format, scientific grade detectors, and review significant progress in achieving higher spatial resolution in large area back-illuminated CCDs. We also present the performance characteristics of a new prototype CCD/CMOS hybrid sensor designed for low light level imaging and capable of high speed, low power, and very low noise.

Keywords: Large format scientific CCD, CCD/CMOS hybrid FPA, low noise, high frame rate, MTF, wafer scale

1. INTRODUCTION

Fairchild Imaging manufactures the largest commercially available CCD detectors with active areas larger than 80 x 80 mm². These wafer scale devices are designed for various aerospace, medical and scientific applications. They can be optimized for very high resolution with pixel dimensions as small as 8.75 μm x 8.75 μm, or for very high sensitivity with large pixel area (up to 39 μm x 39 μm), and full well capacities exceeding one million electrons. Fairchild Imaging has produced several thousand wafer scale imagers for use in sophisticated imaging applications such as astronomy, medical x-ray imaging, x-ray crystallography, electron microscopy, aerial reconnaissance, and space observation [1].

Fairchild Imaging has developed a reliable thinning process that enables routine production of back-illuminated, full frame 4k x 4k CCD detectors featuring an active area of 60 x 60 mm². The manufacturing process has matured to the point where devices of exceptional cosmetic quality can be completed with high yield in a relatively short cycle time of weeks rather than months. We will present the results of recent technological developments aimed at improving the spatial resolution of these large area detectors.

We will also describe a new detector architecture that combines the best of CCD characteristics (i.e., high quantum efficiency, low dark current, low fixed pattern noise, and low cross talk) with the high speed, low power and ultra-low read noise capabilities of CMOS technology. This hybrid approach provides clear benefits to a number of demanding imaging applications in scientific, medical and defense imaging systems that require low-light image sensors capable of high sensitivity and low noise performance at very high frame rates. Other potential applications include wavefront sensing for adaptive optics (AO), and synchrotron x-ray diffraction analysis.

2. LARGE AREA SCIENTIFIC DETECTORS

2.1. Wafer-scale CCD detectors

The size of the CCD detector plays a critical role in the imaging system performance since it essentially defines the field of view of the system. Our 4k x 4k CCD486 measures 60 mm per side because the device was initially designed to replace medium format film used in professional photography applications. The 9k x 9k CCD595 measures 80 mm per side, the device was originally designed for aerial reconnaissance applications where maximum resolution and wide field of view are the key requirements. To date, Fairchild Imaging is still the only commercial CCD manufacturer to produce wafer scale detectors in large volume. In order to manufacture monolithic image sensors with active areas that cover most of the usable area of a 125 mm diameter wafer, many design and process refinements are necessary. A

detailed description of our wafer fabrication technology is available in previously published proceedings of SPIE [2]. A summary of our current wafer scale CCD detectors is shown in Table 1 below.

Table 1. Large format CCD focal plane arrays

CCD part number	Format H x V (pixels)	Pixel size (μm^2)	Imaging area (H x V, mm)	Features
CCD485	4k x 4k	15 x 15	61.20 x 61.21	Frontside, 3-phase, MPP, 4 outputs
CCD486	4k x 4k	15 x 15	61.44 x 61.45	Front or back-illumination, 4 outputs
CCD595	9k x 9k	8.75 x 8.75	80.64 x 80.64	Frontside, eight 25-MHz outputs
CCD8161	4k x 4k	19.5 x 19.5	79.87 x 79.87	Frontside, 3-side butting, 4 low-noise and 4 high-speed outputs
CCD582	12k x 128	8.75 x 8.75	107.52 x 1.12	Frontside, bi-directional TDI sensor with 128 selectable TDI stages and 8 high speed output ports

2.2. Back-Illuminated 16-Megapixel CCD with improved MTF

Conventional front-illuminated CCDs have poor quantum efficiency at short wavelengths since the photon absorption depth in silicon is very shallow ($\sim 0.2 \mu\text{m}$ @ 400 nm), therefore the incident radiation is nearly completely absorbed as it passes through the various layers of materials present on the surface of the CCD. This undesirable situation can be avoided and a dramatic improvement in QE can be obtained by thinning the CCD, and allowing the incident light to interact directly with the bare and featureless backside surface of the CCD.

Back-illuminated CCDs typically suffer from degradation in spatial resolution at short wavelengths, due to carrier lateral diffusion in the field-free region between the back surface and the depletion region. This effect can be minimized by fabricating the device on high resistivity material to extend the edge of the depletion region, but this approach often leads to increased dark current because of the thicker active volume, and also because the material tends to be of lower quality. We implemented an alternate approach which involves controlling the thickness of the CCD so that the distance between the edge of the depletion region and the point where the charge is generated is less than the pixel pitch. This condition significantly improves the sensor spatial resolution since the carriers now reach the depletion region before they have a chance to diffuse laterally to neighboring pixels [3].

We thinned the CCD486, a 4k x 4k CCD with 15 μm pixels, to a final thickness of 10 μm , which produced a distinct improvement in MTF, and still provides acceptable red QE. The spectral response curves shown in Figure 1 are produced by devices thinned to 10 μm with anti-reflection coatings optimized for blue-enhanced (430 nm) and broadband (650 nm) response. The QE curve of the standard 20- μm thick CCD486 with the blue-enhanced anti-reflection coating is also shown for comparison. While the QE of the 20- μm thick device is higher above 650 nm, it comes with a performance tradeoff in terms of lower MTF at short wavelengths. The 10- μm thick active layer results in a definite improvement in MTF since at normal operating voltages, the edge of the depletion region extends to about 5 μm below the surface of the CCD, leaving a field free region of only 5 μm , which is significantly less than the pixel-to-pixel spacing of 15 μm .

2.3. MTF measurements

To characterize the spatial resolution of the device, we measured its MTF at 410 nm where the photon absorption length is less than 0.2 μm . The MTF test setup is shown in Figure 2. The CCD is mounted in the camera and cooled to -60°C , and the slanted edge target is projected onto the CCD using a long working distance microscope objective. The MTF calculations are performed according to the guidelines described in ISO Standard 12233. At the Nyquist frequency, or 33.3 lp/mm, the MTF is better than 30%. The measured MTF curve is shown in Figure 3.

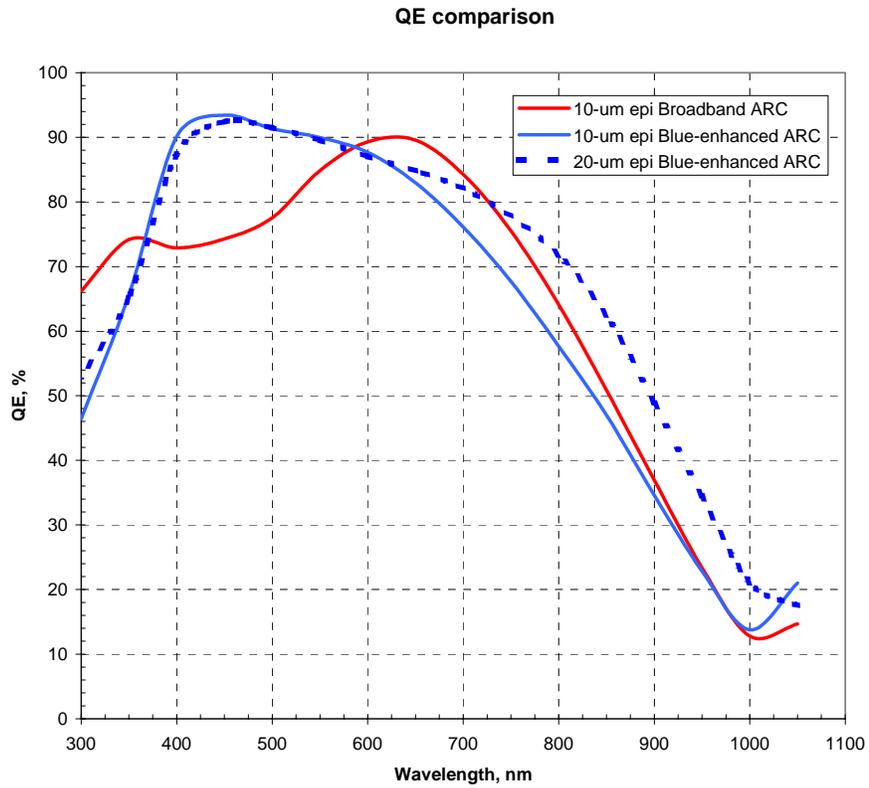


Figure 1. Back-illuminated CCD486 QE curves

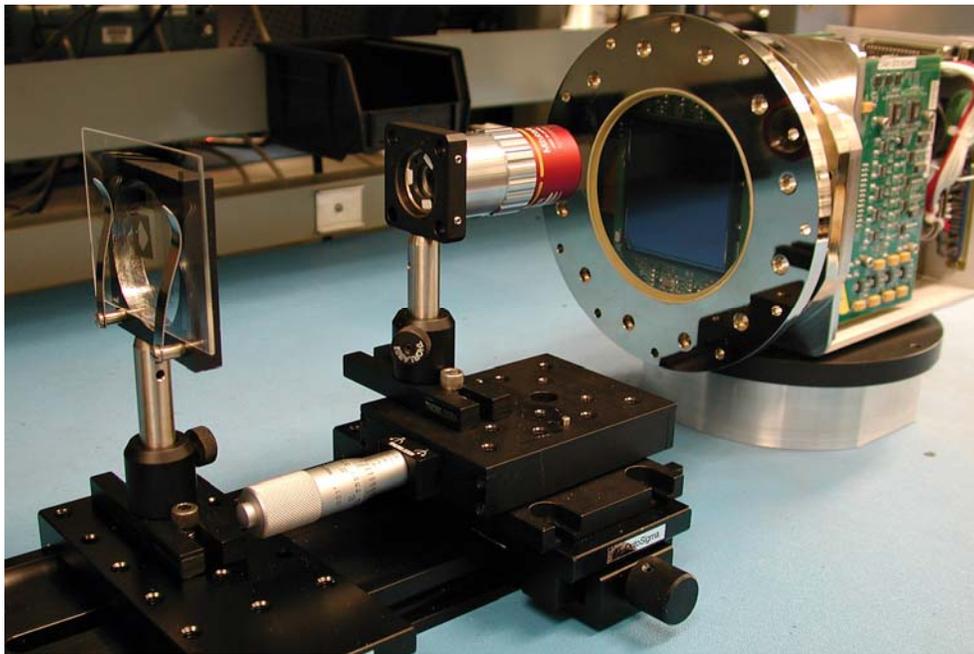


Figure 2. Simplified illustration of the MTF test setup (not shown are the light baffle, light source, and diffuser)

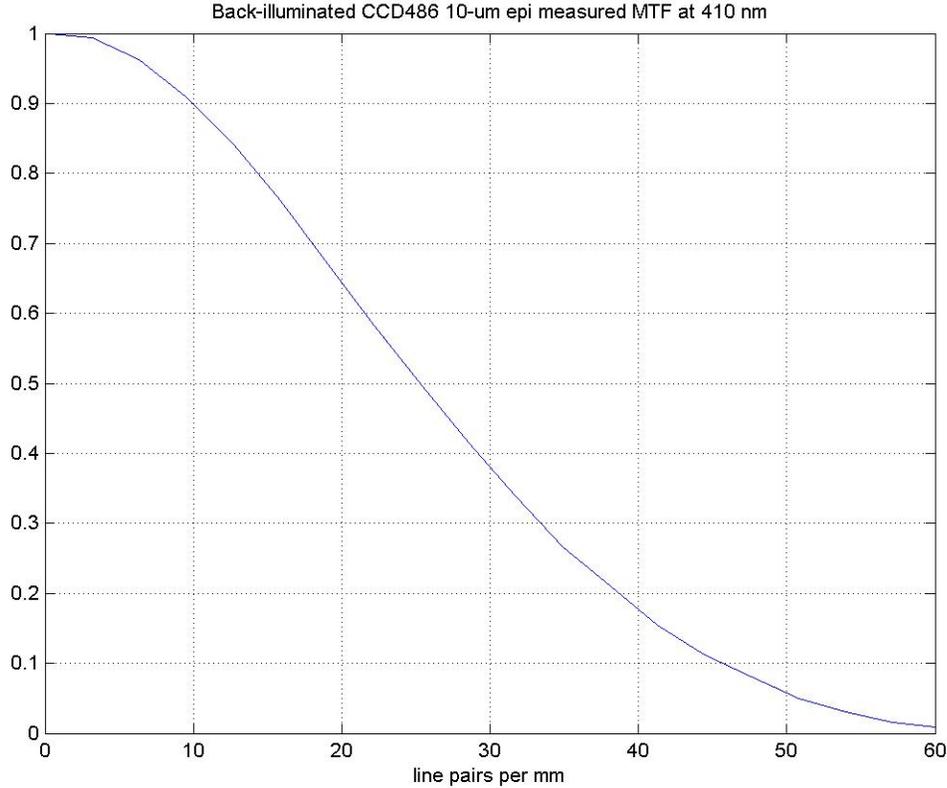


Figure 3. MTF of 10 um back-illuminated CCD486 at 410 nm, Nyquist frequency = 33 lp/mm

3. CCD/CMOS HYBRID IMAGE SENSOR

3.1. Hybrid image sensor architecture

Modern CCD imagers deliver exceptional image qualities with near ideal quantum efficiency (QE), low dark current (<10 pA/cm² at room temperature), high linearity and response uniformity. However, one of the main shortcomings of conventional CCDs is the relatively long readout times since each row of pixels must be read out serially using a limited number of output amplifiers. In a large format CCD, the amplifiers need to be operated at wide bandwidth to support high frame rates, so the read noise significantly increases, and the CCD performance is compromised. For example, for a 1k x 1k CCD with 4 output amplifiers running at 30 frames per second, its amplifiers need to be operated at 7.5MHz, causing the read noise to increase to 14 – 15 e- RMS. The high-speed serial shift registers and the output amplifiers also contribute to high power consumption.

In our hybrid sensor approach, the charge signal is transferred out of the CCD to a low noise CMOS readout circuit at the end of each column, and the normal width serial shift registers are eliminated, which significantly improves the data throughput. In a multi-megapixel sensor, the column parallel readout architecture can potentially result in up to 3 orders of magnitude in improved frame rate.

Depending on the applications and hardware requirements, a wide variety of CCD architectures can be implemented in a hybrid sensor. In addition to a frame interline transfer CCD, other suitable devices include frame transfer (FT), and TDI arrays, both in frontside and backside illuminated formats.

The hybrid sensor consists of two CMOS ROICs bonded to a CCD focal plane array. Note that the CCD does not contain any on-chip amplifiers. During readout, the charge collected in each pixel is vertically shifted to the end of each column, to be subsequently transferred across an indium bump bond into the CMOS ROIC. Each ROIC contains an array of low noise capacitive transimpedance amplifiers (CTIA) [4] which are connected to floating diffusion sense nodes on the CCD via indium bump interconnects. The CTIA converts the CCD charge signal into a voltage and amplifies it with very high gain. The column parallel layout of the CTIA allows it to fill a large area in the column direction which allows for a sophisticated amplifier design. The ROIC also contains circuitry to perform correlated double sampling (CDS) and multiplexing operations. In future designs, on-chip analog to digital conversion (ADC), timing generation, digital control and image processing can also be integrated on-chip to further improve the performance of the sensor.

In this approach, the bandwidth of the CTIA is roughly half the reciprocal of the CCD line time, which is orders of magnitude lower than the requirement of a conventional CCD output amplifier. The parallel architecture offers clear benefits in improved speed and reduced noise: Sensors of moderate format can operate at thousands of frames per second, larger format sensors can run at hundreds of frames per second, and extremely low noise can be achieved at normal video rate.

3.2. Noise analysis

Since there are no on-chip amplifiers in the CCD, the dominant noise source in the hybrid FPA is the CTIA. Figure 4 shows the CTIA noise model used in the analysis. In this model, C_{in} is the input capacitance that includes CTIA input transistor gate capacitance, CCD output node parasitic capacitance, and any parasitic capacitance associated with the indium bump; C_{fb} is the CTIA feedback capacitor; C_{load} is the CTIA band limiting capacitor.

The input referred amplifier noise power spectral density $V_n(f)$ contains both the thermal noise and 1/f noise components,

$$|V_n(f)|^2 = \frac{8kT}{3g_m} + \frac{K_f g_m^2}{f^{A_f}} \quad (1)$$

where g_m is the transconductance of the amplifier and K_f , A_f are the 1/f noise parameters. Assuming that the CDS operation eliminates most of the 1/f noise, the input referred noise (N) in e- RMS can be simplified as:

$$N \approx \sqrt{\frac{8kT}{3g_m q^2} \cdot NBW \cdot C_{in}^2} \quad (2)$$

where NBW is the CTIA close-loop noise bandwidth, i.e., $NBW = \frac{\pi}{2} BW_{Amplifier}$

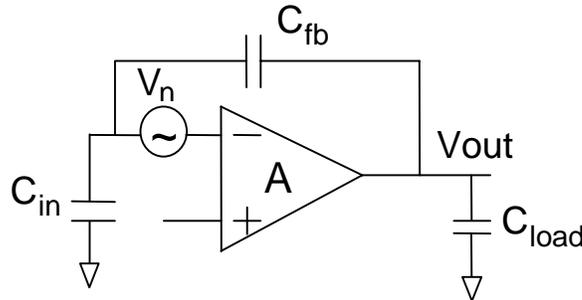


Figure 4. CTIA noise model

The above equation clearly demonstrates that the input referred noise is proportional to the square root of the CTIA bandwidth. Also note that the noise increases with the input capacitance C_{in} , hence it is critical to keep the parasitic capacitance at the CCD output node and indium bump as small as possible.

Figure 5 shows the predicted noise vs. frame rate for an 1k x 1k hybrid sensor assuming a bump capacitance of 40fF, and Figure 6 shows the predicted noise vs. number of rows (i.e. active lines) for a sensor operating at 30 frames/sec.

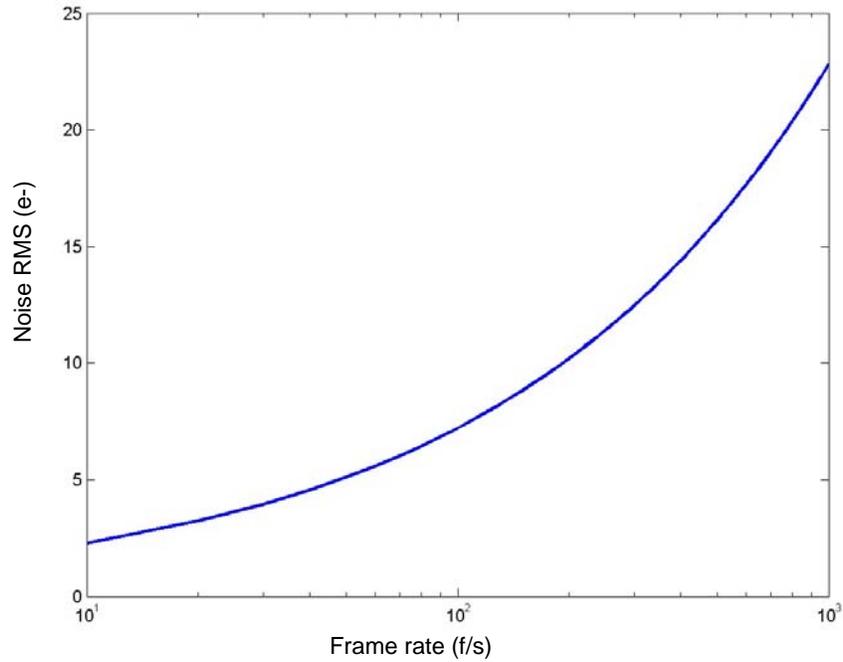


Figure 5. Predicted noise vs. frame rate

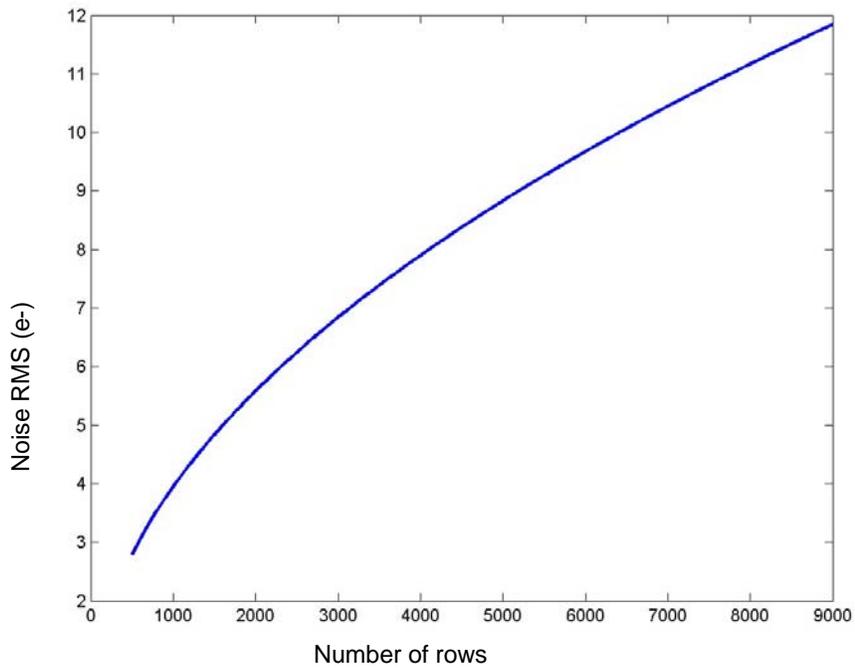


Figure 6. Predicted noise vs. number of rows at 30 frames/sec

3.3. Performance of the prototype hybrid sensor

The prototype hybrid sensor [5] was completed in mid-2005, and consists of a split frame transfer CCD of 1280(H) x 1024(V) array dimensions with 12 μm square pixels. The CCD vertical registers are 2-phase to facilitate pseudo-interlaced video operation. The CCD was also designed to accommodate on-chip charge binning operations for improved SNR and increased frame rate performance, with a slight trade-off in spatial resolution. Mini serial registers are placed at the end of each group of 4 columns, and terminated with a floating diffusion sense node. Indium bumps are used to establish electrical connection between the CCD and the CMOS ROIC. In addition to its role as a photon detector, the CCD also serves as a support handle for the CMOS readout chips. The CMOS I/O pads are connected to the CCD using indium bumps, and all connections to the package of the sensor are established through bonding pads located on the CCD. The packaged CCD/CMOS hybrid sensor is shown in Figure 7.

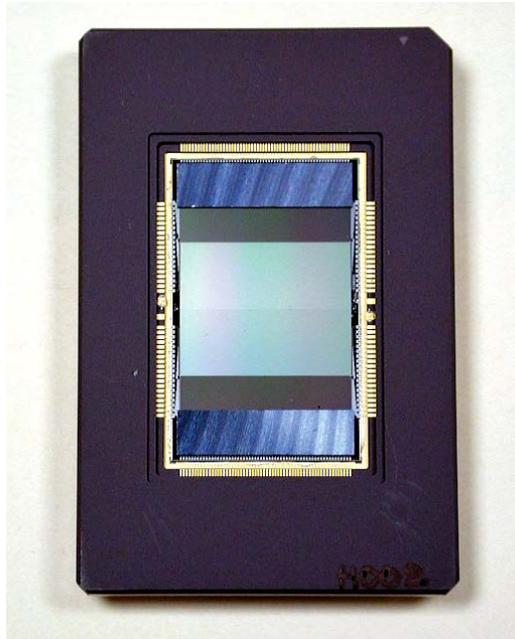


Figure 7. Hybrid CCD/CMOS sensor assembly

The CMOS ROICs are based on 0.35 μm 1P4M process technology, and operate at 3.3V. Charge to voltage conversion is performed in the ROIC using an array of low fixed pattern noise capacitive transimpedance amplifiers that feature selectable high or low gain operation. The readout circuitry also accommodates true correlated double sampling (CDS), adjustable speed depending on the binning mode, and contains circuits for controlling analog bias, timing generation and multiplexing. The data output is multiplexed and read out through two output ports in each ROIC. The sensor is designed to operate at 30 Hz frame rate, and the data output rate per port is 16 MHz.

The hybrid sensor is mounted in a custom ceramic package and integrated into a compact camera which holds 3 boards: the sensor board, the driver and digitization board, and a digital camera control board. The camera uses the Cameralink interface.

The device characteristics are summarized in Table 2. At 30 Hz frame rate, the readout noise is as low as 2.9 e^- , while the sensor average total noise (readout noise and thermal noise summed in quadrature) is 6 e^- rms. While this value is higher than our design goals and predictions, we have identified that it is partly caused by a large indium bump capacitance and resultant lower conversion gain. There were some process related issues during the early phase of development that resulted in oversized indium bumps being deposited on the devices. These issues have been successfully resolved, and tighter bump dimensions, as well as improvements in the bump formation and the hybridization processes, are expected to reduce the bump capacitance and lower the readout noise of subsequent devices.

Table 2. Prototype hybrid sensor characteristics

H1011 Characteristics

Format	1280(H) x 1024(V)
Pixel size	12 x 12 μm^2
Spectral range	400 - 1100 nm
Peak QE	40%
Conversion gain	160 uV/e-
Non-linearity	<1%
Dynamic range	high gain mode = 2000:1 low gain mode = 6000:1
Dark current at 23 °C	6 - 8 pA/cm ²
Smear at full saturation	0.05%
Outputs	4 (multiplexed)
Frame rate	1x1 unbinned 30 fps 2x2 binned 52 fps 4x4 binned 128 fps

4. CONCLUSIONS

Fairchild Imaging continues to develop new technologies in order to further improve the performance of its product line and to meet the increasing demands for higher resolution, higher speed, and lower noise. In this paper, we have presented some examples of these efforts and their promising results. While we continue to expand the capabilities of our proven wafer scale CCD technology, we are also developing advanced high speed CMOS image sensors, as well as combining the best of the two technologies to produce hybrid image sensors that are capable of uncompromised performance.

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